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Overcoming the Minimum V_{DD} Ramp Rate Limitation of the ISL25700

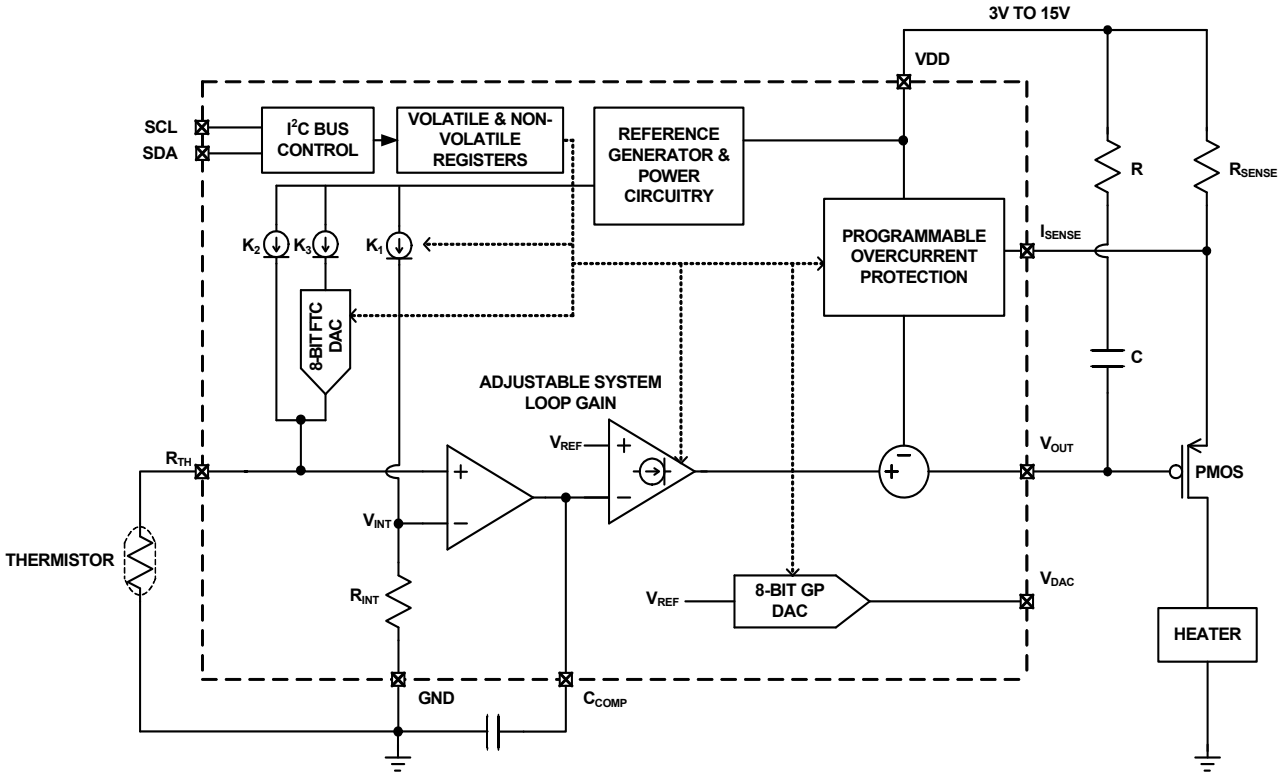
Background

The ISL25700 is a Temperature Controlled MOSFET Driver that is an integral part of a temperature control loop to maintain a constant pre-programmed temperature for many applications but is primarily used in Oven Controlled Oscillators or OCXOs.

It features a programmable overcurrent protection of the MOSFET that automatically adjusts the output voltage in order to keep the MOSFET power under user defined limits.

The protection settings always override the temperature settings that cause violation of the current limit. These settings are all programmed and stored in non-volatile memory.

Block Diagram/Application Circuit



V_{DD} Ramp Rate Limitations

The ISL25700 datasheet specifies a parameter called "V_{DD} Ramp Rate" with a minimum of 0.2V/ms and a maximum of 50V/ms as its limits. Table 1 shows an excerpt of the Operating Specifications table pertaining to this specification. The outcome of violating the specification is data corruption of the non-volatile memory. This corruption causes the memory to be reset to a baseline state and can cause damage to the ISL25700 or the MOSFET.

While the datasheet specifies that this ramp rate must be adhered to from 0V to 15V, it has been shown in lab testing to be only critical from 0V to the minimum operating voltage, 3V. Once the ISL25700 V_{DD} voltage reaches 3V, the ramp rate can violate the spec and non-volatile memory will be retained. In fact, there is some margin below 3V. Empirical testing has shown that once V_{DD} reaches approximately 2.5V, memory will be retained.

TABLE 1. V_{DD} RAMP RATE SPECIFICATION

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD} Ramp	V_{DD} Ramp Rate	@ Any Level From 0V to 15V	0.2		50	V/ms

In normal OCXO applications, V_{DD} ramp rates are not usually a problem and fall somewhere between the minimum and maximum; however, during evaluation, OCXOs are commonly ramped up by hand on a bench supply. Doing so will almost certainly result in memory loss. Exceeding the maximum V_{DD} ramp is usually not an issue, however, if it were to become an issue, it can be easily solved by adding more decoupling capacitance to slow down the ramp rate.

The Solution

Since the most critical voltage range for memory loss caused by slow ramp rate is between 0V and 3V, the easiest solution is to hold off V_{DD} from being applied to the ISL25700 and the P-channel MOSFET until V_{DD} has reached the 3V threshold.

Figure 1 shows a circuit that achieves this desired outcome. The ISL88001 is a Power On Reset/Voltage Monitor IC. It has an active low reset output that powers up low (0V) and remains low as long as V_{IN} is <2.92V nominal. As soon as 2.92V is reached, the reset of the output goes high (V_{IN}). It will track V_{IN} until the zener diode D1, reaches its breakdown voltage of approximately 5.1V and then levels off at near to that voltage. The zener is needed because the maximum operating supply voltage of the ISL88001 is 5.5V. It draws very little quiescent current (400nA max), so a zener diode is ideal. PLVA650A was chosen for its small size, low reverse leakage and low cost.

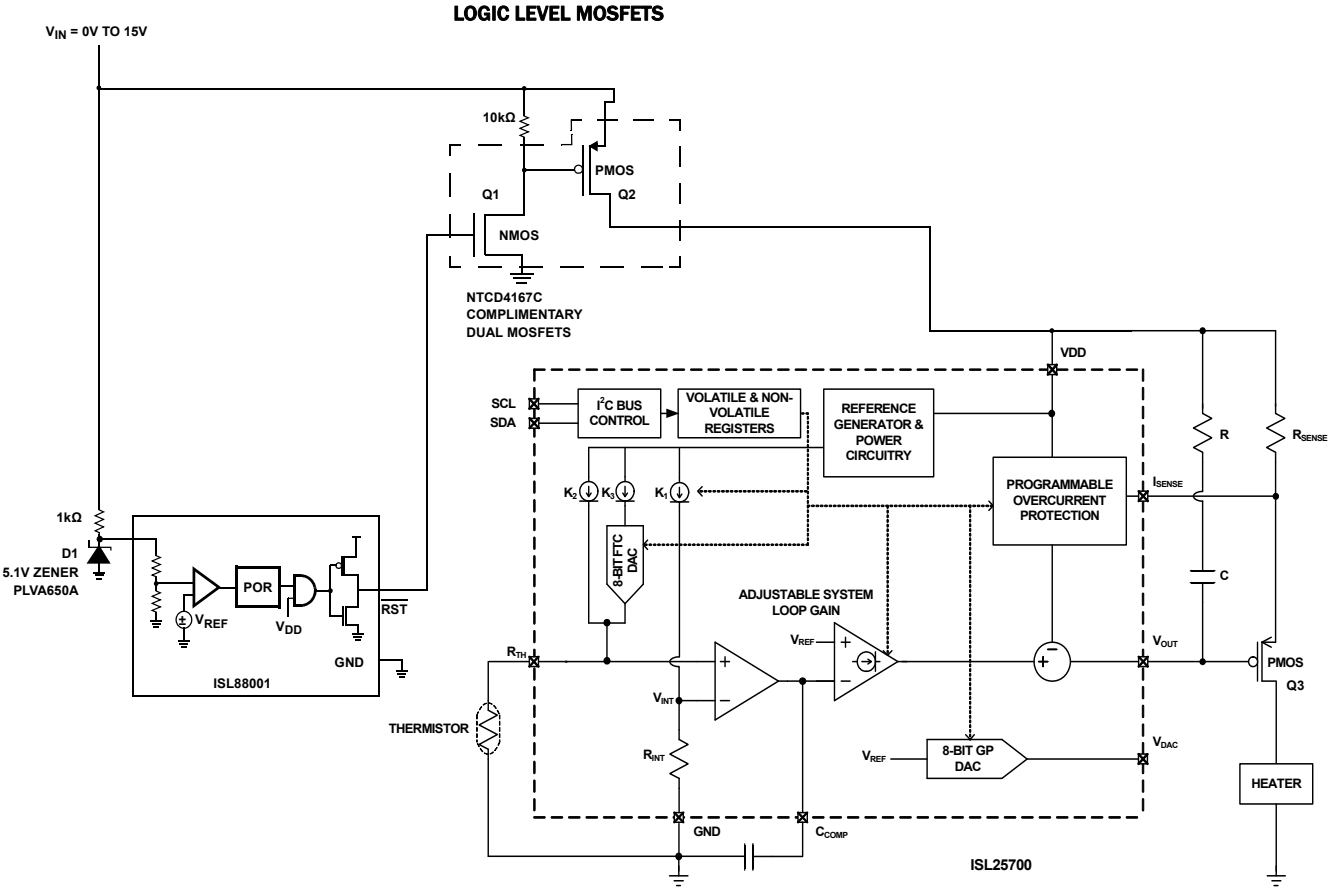


FIGURE 1. V_{DD} HOLD OFF CIRCUIT

Once V_{IN} reaches ~2.92V, the reset output goes high and turns on the N-channel MOSFET, Q1, which in turn turns on the P-channel MOSFET, Q2, and allows V_{IN} to be applied to both the ISL25700 and the controlled P-channel MOSFET, Q3. A dual complimentary MOSFET pair, NTGD4167C, was used for testing the circuit due to the small size, low cost and good $r_{DS(ON)}$ performance. Any heating in the MOSFET pair will be compensated by the ISL25700.

Figure 2 is an oscilloscope shot of the resulting circuit's waveforms. V_{IN} (Blue) is allowed to ramp slowly to 15V at a rate slower than the minimum 0.2V/ms. It is held off by the ISL88001 until V_{IN} reaches ~2.92V. In this case, by the time V_{IN} reaches the threshold and the Gate of the N-channel FET (Purple) causes Q1 to turn on, V_{IN} has already reached ~11.5V and is applied to the ISL25700 and Q3 (Green). No non-volatile memory loss was noted.

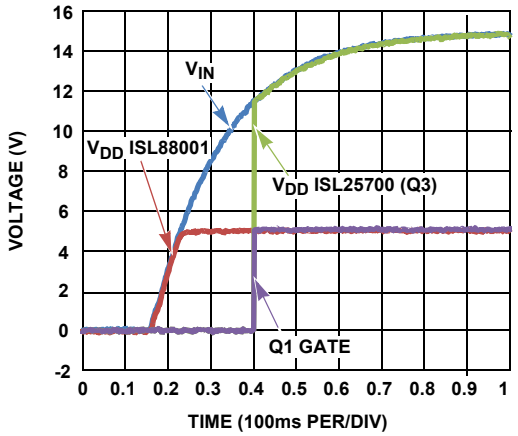


FIGURE 2. SCOPE SHOT OF HOLD OFF CIRCUIT WAVEFORMS (V_{IN} RAMPS 0V TO 15V)

In order to verify that V_{IN} is being held off till it reaches ~2.92V, the experiment was repeated but V_{IN} was limited to a maximum of 3.1V. Figure 3 shows the resulting waveforms. It is clear that V_{IN} is held off from being applied to the ISL25700 and Q3 until after the threshold is reached. No non-volatile memory loss was noted.

This experiment was also repeated for a third and final time but this time V_{DD} was very slowly ramped by hand to verify that having a threshold of ~2.92V would not cause any memory loss issues.

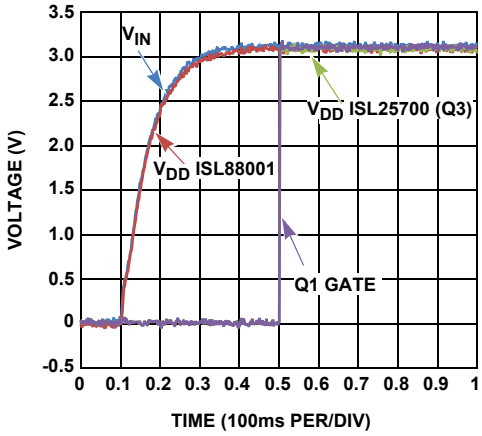


FIGURE 3. SCOPE SHOT OF HOLD OFF CIRCUIT WAVEFORMS (V_{IN} RAMPS 0V TO 3.1V)

Conclusions

It has been confirmed in the lab that the ISL25700 will have non-volatile memory loss issues if the min and max ramp rates are violated which could result in circuit damage. The only time memory loss was confirmed was from 0V to 3V.

In most OCXO applications, the actual ramp rate will fall between the minimum and maximum limit, however, the minimum ramp rate can often be violated in evaluation in the lab. It is recommended that a V_{DD} hold off circuit, similar to Figure 1, be implemented to prevent memory loss and/or circuit damage.